Effect of Substrate Bias in the Capacitive Coupling of SOI UTBB MOSFETs

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***Abstract*— In this work, the electrical features related to the capacitive coupling of the Ultra-Thin Body and Buried Oxide SOI MOSFET (UTBB) transistors is explored through numerical simulations. The impact of the substrate bias is observed for a set of values ranging to -3V for 2V. Also, structures of with different types of ground plane (GP-P and GP-N) and without GP has been evaluated. This approach analyzes the capacitive coupling through the Body Factor and shows that the negative biasing for all GP types significantly improves the structure coupling and that the device with P-type ground plane has the lowest value of Body Factor for all the evaluated conditions.**

Keywords- Substrate Bias, UTBB, Capcitive coupling, Body Factor

INTRODUCTION

The continuous demands of increasing the integration density of the integrated circuits has led to the exponential reduction on the MOSFETs dimensions since the middle of the 60`s [1]. However, along the last decades, the reduction in the devices dimensions has been inefficient due to the occurrence of unwanted effects such as large parasitic currents and capacitances. These phenomena are related to short channel effects (SCEs) [2,3,4], which tend to appear at extremely reduced dimensions. So that, it has been necessary to develop novel technologies such as the SOI-MOSFET that consists in a MOSFET structure with the active silicon channel layer isolated from the wafer substrate by a buried oxide layer (BOX) [2].

This structure presents a large reduction in SCEs with respect to the conventional (or bulk) MOSFET technology as well as inherently reduced parasitic effects due to channel insulation. However, for ultra-submicrometer devices even devices fabricated in conventional SOI technology exhibit strong SCEs [4]. For that reason, some improvements have been proposed. Initially, it was proposed the reduction of the silicon layer in order to enhance the capacitive coupling of the structure (Ultra Thin Body transistor - UTB). However, for small devices, the thin silicon above a thick buried oxide can bring some drawbacks such as the self-heating, once the BOX layer present low thermal coefficient and harms the heat removal of the silicon channel [5,6,7].

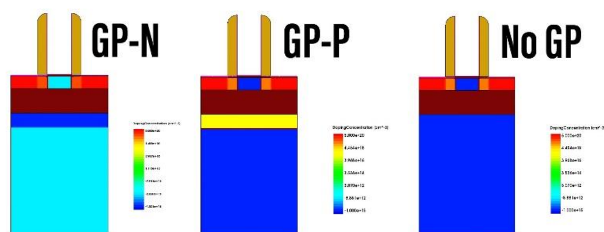

Figure.1 – Three SOI UTBB transistor with L=20nm; tsi=10nm, tbox=20nm and Ground Plane type P, type n and no GP.

In the sequence, as an evolution of the UTB devices, it was proposed a transistor in which both the silicon and the buried oxide layer were reduced. This device has been called UTBB (Ultra Thin Body and Buried Oxide) SOI MOSFET and its schematic is shown in Figure 1. Due to the small thickness of the BOX layer (10-20 nm) [8,9,10], it can be used as a second gate for the transistor, improving the capacitive coupling of the structure. Both top and bottom gates are independent, such that the potential applied to the substrate (V_{BS}) can be adjusted to improve the devices characteristics. Usually, a negative potential applied to the substrate reduces the leakage whereas a positive bias makes the device faster, since the threshold voltage can be modulated by the variation of V_{BS}. In order to enhance the effect of the V_{BS} application as well as to allow the access of the substrate of individual transistors, a highly doped thin silicon layer is created below the BOX layer, which is called ground plane (GP) [11]. This layer can present with N- or P-type doping concentration as also shown in Figure 1.

However, the variation of V_{BS} changes the capacitive coupling of the structure, affecting the subthreshold swing as well as the current capability of the devices. For that reason, this work will verify the behavior of the UTBB-SOI-MOSFET capacitive coupling when its substrate is biased from -3 V up to 2 V for structures with N- and P-type GPs and without GP. The analysis has been performed for a channel length range of 20nm to 500nm.

DEVICES AND SIMULATIONS CHARACTERISTICS

The analysis of the substrate biasing on capacitive coupling in UTBB SOI-MOSFET transistor was performed through 2D numerical simulations performed in Sentaurus Device TCAD[12], this software was chosen because of its well-known robustness and its simulation format that consist in a grid points that allows the construction and simulation of any structure.

Along the simulations, the devices were defined with silicon channel thickness (t_{si}) of 10nm, top gate oxide thickness (t_{ox}) of 1.7 nm, buried oxide thickness (t_{box}) of 20 nm, drain and source lengths (L_{fd}) of 30nm, channel length ranging from 20 nm to 500 nm, source and drain arsenic doping concentration of 5×10^{20} cm^{-3} and channel and substrate

boron doping concentration of 1×10^{15} cm^{-3} . The ground plane presents thickness (t_{gp}) of 10nm and presents doping concentration of 1×10^{19} cm^{-3} and 1×10^{18} cm^{-3} for the P- and N-type GP, respectively. All the devices characteristics were chosen based on the UTBB structure described in [10], proposed by STMicroelectronics.

The simulation performed in Sentaurus account for models considering the effects of the mobility degradation through vertical and longitudinal electrical fields, bandgap narrowing, carriers` generation and recombination and quantum confinement. The overall analysis was performed for V_{GS} ranging from -0.5 V to 1.2 V, V_{BS} ranging from -3 V to 2 V and V_{DS} = 50 mV.

CAPACITIVE COUPLING ANALYSIS

The first step of the analysis consisted in the simulation of the drain current (I_{DS}) curves as a function of the gate voltage for the devices with and without ground plane biased at V_{DS} = 50 mV and V_{BS} = 0 V for different channel lengths (L). In Figures 2 (A) and (B), we can see the simulated I_{DS} curves in linear and logarithmic scales, respectively. In Fig. 2(A), it is possible to see a dependency of drain current with the channel length, in which a reduction in L promotes an I_{DS} increase as well as a lowering of V_{TH} due to the occurrence of SCEs. Considering a same L and a fixed bias, a larger current is observed for the N-type ground plane device. In Fig 2 (B), it is possible to observe the degradation of the subthreshold of the devices for L ≤ 50 nm due to the SCEs.

In order to evaluate the capacitive coupling of the structure, the subthreshold swing (SS) of the devices was obtained for different substrate biases. This parameter represents the variation of V_{GS} needed to shift I_{DS} in one order of magnitude. SS can be directly extracted from I_{DS} x V_{GS} curves by derivative of the inverse of the logarithm of I_{DS} as a function of V_{GS}. The curves of the subthreshold swing are exhibited in Figure 3 as a function of the channel length for different substrate bias. We can see a nearly exponential trend of SS as the channel length decreases, which can be associated to the to the intensification of the short channel effects that cause the control loss of part of the depletion region by the gate [13,14], thus varyng the capacitive coupling.

By the ground plane point of view, we can only notice a diference when the channel length decreases below of 100nm where the p-type ground plane presents slightly smaller values, which coould be related to the capacitive coupling of the structure. In this figure it is also possible to observe that as more negative is the substrate biasing, lower is the subthreshold slope. The negative Vbs tends to lead the interface between silicon and buried oxide to the accumulation. In this case, the current flows closer to the gate dielectric interface and the top gate presents a better control over the channel charge.

To better understand the behavior of the drain current and subthreshold swing with respect to the capacitances of silicon and gate oxide, SS can be written according to expression (1), which associates the subthrehold slope to the body factor (α).

$$SS = \frac{kT}{q} \ln(10)(1+\alpha) \qquad (1)$$

Where T is the temperature. The body factor is used to measure variation in threshold voltage due to substrate biasing and it can also be associated to the variation of the surface potentials and, consequently, the variation of the capacitive coupling on device and as smaller its value, the higher is the quality factor. The boby factor in an SOI fully depleted device is given by expression (2) [2].

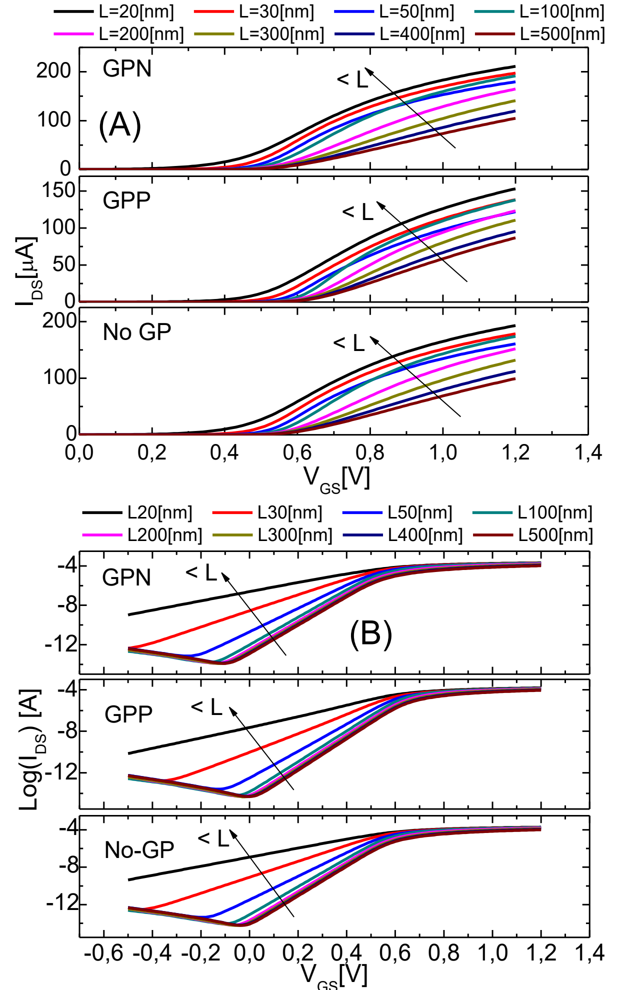

Figure. 2 Drain current as a function of gate voltage for three settings of ground plane and V_{BS} = 0 V in linear (A) logarithmic (B) scales.

$$\alpha = \frac{C_{Si} C_{OX2}}{C_{OX1}(C_{Si}+C_{OX2})} \qquad (2)$$

The body factor in a fully depleted device is approximately given by the ratio between the series assossiation between the silicon and buried oxide capacitances (C_{Si} and C_{OX2}, respectively) by the gate oxide capacitance (C_{OX1}). For very thin silicon layers, such as in the case of the UTBB, the point of the silicon layer in which the centroid of charge is located, i.e. the point where there is the highest concentration of electrons becomes important. So

that, expression (2) must be rewritten in terms of the position of the centroid of charge (Xbar), as shown in (3) [15].

$$\alpha = \frac{t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_{si}}(X_{bar})}{t_{box}+\frac{\varepsilon_{ox}}{\varepsilon_{si}}(t_{si}-X_{bar})} \quad (3)$$

where ε_{ox} and ε_{Si} are the permitivitties of the oxide and silicon respectively.

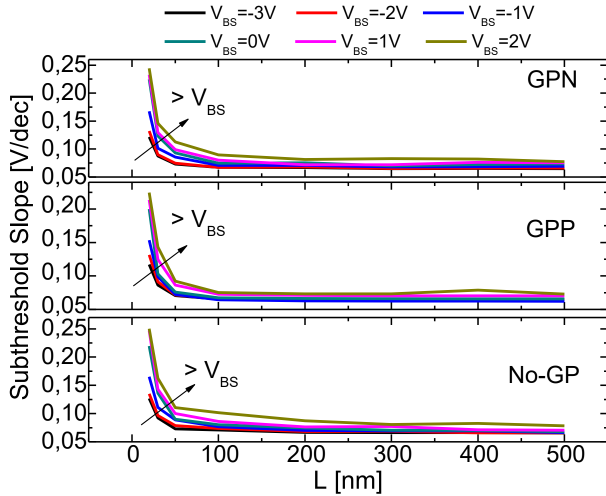

Figure. 3. Subthreshold slope as a function of the channel length for devices with N- and P-type GPs and without GP for V_{BS} ranging from -3v to 2v.

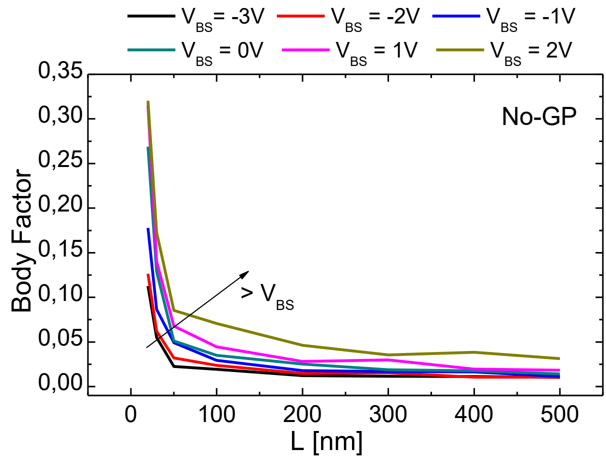

Figure. 4 Body factor as a function of channel length for devices without GP for V_{BS} ranging from -3V to 2 V.

When the body factor is presented as a function of the channel length as in Figure 4, we observe the same trend presented on the analyses of the Figure 3. The smaller the channel length, higher is the body factor presented. Due to the occurrence of short channel effects, the depletion charge controlled by the gate is reduced, affecting the silicon capacitance and increasing the body factor. This effect can be understood through expression 2.

As we can see in Figure 4, and mainly in Figure 5, which shows the body factor as a function of the substrate bias for all channel lengths evaluated for devices without GP. a lower body factor, i.e. better capacitive coupling, is noticed as more negative is the substrate biasing.

This effect can be explained through expression (3). As the substrate bias is reduced, the electrons inside the silicon layer are pushed to the upper part of the channel, closer to the interface with the gate oxide. In this case the centroid of charge is close to the top interface, resulting in a small value for Xbar, which induces a smaller α. As the substrate bias is increased, part of the electrons is pushed down to the back interface, moving the centroid deeper inside the silicon layer and increasing Xbar, which results in an increment of the body factor.

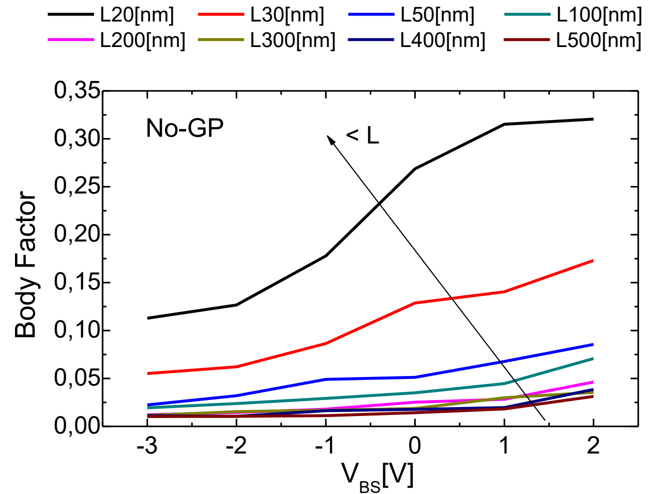

Figure. 5 Body factor as a function of substrate bias for devices with channel length ranging from 20 nm to 500 nm.

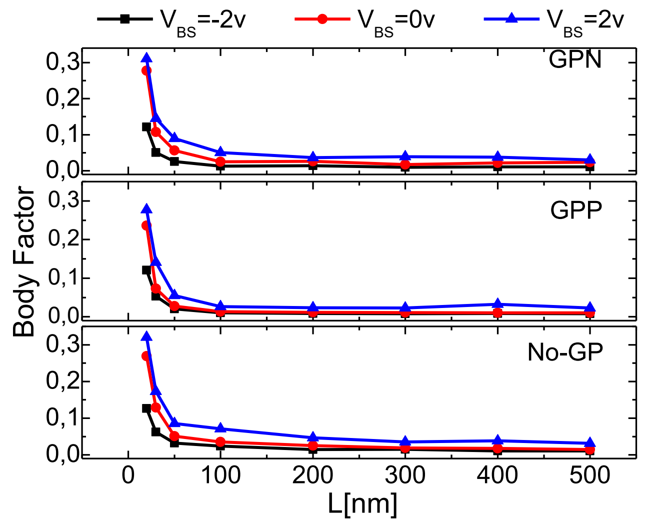

Figure. 6 Body factor as a function of channel length ranging from 20nm to 500nm for three setings of ground plane and V_{BS} ranging from -3v to 2v.

Figure 6 presents the body factor as a function of the channel length for devices with N- and P-type ground planes and without ground plane biased at V_{BS} = -2 V, 0 V and 2 V. It is possible to perceive that contrarily to the strong variation in the body factor promoted by the substrate biasing, the

ground plane does not make a large diference in the capacitive coupling.

In order to better observeed the impact of the GP in the body factor of the devices, Figure 7 presents with more distinction the effect in capacitive coupling of the substrate biasing and ground plane implantation for any channel length. In this figure, it is possible to see that for more negative biasing, the effect of ground plane implantation is reduced, i.e. all the devices configurations (P-type, N-type or no GP) present similar body factor. However, for positive substrate bias, the P-type ground plane promotes a reduction in the body body factor. The different body factor are related to the different flatband voltages of the devices. For N-type GP, for example, the flatband occurs at lower gate voltages, which indicates that at a similar biasing condition, such device present a stronger depletion at the second interface.

Anyway, the P-type ground plane presented better values of body factor for all channel lengths as well as, the smaller the channel length, higher the short channel efects and, the greater the short channel efects, more efficient is the negative biasing for reduce them.

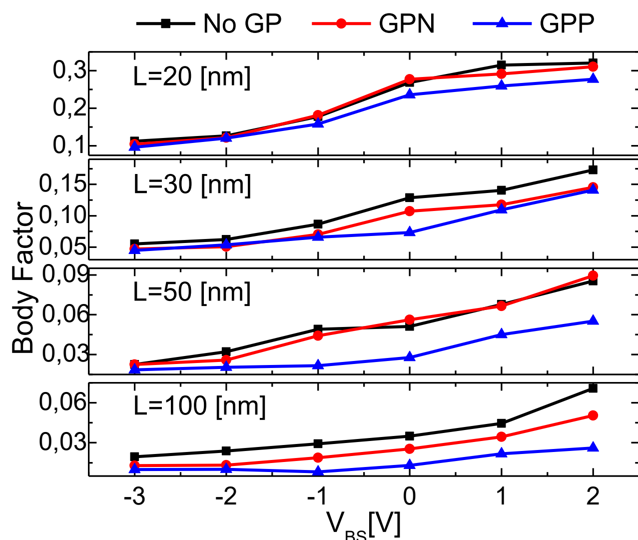

Figure. 7 Body factor as a function of V_{BS} biasing ranging from -3 V to 2 V for channel length ranging from 20nm to 100nm for three setings of ground plane.

CONCLUSIONS

This paper has presented an analyses through 2D numerical simulations of the electrical features on UTBBs SOI MOSFETs related to capacitive coupling when its substrate is biased and when a ground plane layer is implanted in its body. The structures simulated were chosen in order to demonstrate the capacitive coupling response to situations where short channel effects are presented in low, medium and critical intensities as well as the biasing and ground plane settings were chosen in order to fully evaluate the electrostatic responses of the transistors. From the point of view of obtaining a better body factor, the configuration with a ground plane layer with p-type dopants presented a better efficiency for all the channel lengths, although the dependence of the body factor with GP is not very large. On the other hand, the variation presented in the capacitive coupling due to substrate biasing was shown to be noticeable. The body factor has shown to increase for positive substrate biases and keeps nearly constant for negative substrate biases.

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